­**Requirements for Microcontroller IF (Prefix: MCI)**

**Reset Condition:**

MCI\_RES\_001. Module shall not enable read/write transactions when the ‘i\_reset’ input is ‘1’.

**Read Operation:**

1. ‘o\_reg\_data’ shall read the data from ‘i\_reg\_r\_data’ when ‘i\_cs’ and ‘i\_r\_neg\_w’ are both set to ‘1’.
2. Module shall read signal from ‘i\_reg\_ack’ and output through ‘o\_ack’
3. ‘i\_cs’ shall be deasserted and reasserted for next read transaction
4. Module shall read signal from ‘i\_r\_neg\_w’ and output through ‘o\_r\_neg\_w’.
5. ‘o\_rs\_vector[0]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x000’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
6. ‘o\_rs\_vector[1]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x004’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
7. ‘o\_rs\_vector[2]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x008’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
8. ‘o\_rs\_vector[3]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x00C’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
9. ‘o\_rs\_vector[4]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x010’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
10. ‘o\_rs\_vector[5]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x014’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
11. ‘o\_rs\_vector[6]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x018’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
12. ‘o\_rs\_vector[7]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x01C’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
13. ‘o\_rs\_vector[8]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x020’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
14. ‘o\_reg\_data’ shall output ‘0’s when ‘i\_addr’ is ‘0x024’
15. ‘o\_reg\_data’ shall output ‘0’s when ‘i\_addr’ is ‘0x030’
16. ‘o\_reg\_data’ shall output ‘0’s when ‘i\_addr’ is ‘0x034’
17. ‘o\_reg\_data’ shall output ‘0’s when ‘i\_addr’ is ‘0x038’
18. ‘o\_reg\_data’ shall output ‘0’s when ‘i\_addr’ is ‘0x03c’
19. ‘o\_reg\_data’ shall output ‘0’s when ‘i\_addr’ is ‘0x040’
20. ‘o\_reg\_data’ shall output ‘0’s when ‘i\_addr’ is ‘0x044’
21. ‘o\_reg\_data’ shall output ‘0’s when ‘i\_addr’ is ‘0x048’
22. ‘o\_reg\_data’ shall output ‘0’s when ‘i\_addr’ is ‘0x04c’
23. ‘o\_rs\_vector[18]’ shall be set to 1 when ‘i\_addr’ is ‘0x050’
24. ‘o\_rs\_vector[19]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x054’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
25. ‘o\_rs\_vector[20]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x058’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
26. ‘o\_rs\_vector[21]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x05C’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
27. ‘o\_rs\_vector[22]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x060’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
28. ‘o\_rs\_vector[23]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x064’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
29. ‘o\_rs\_vector[24]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x068’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
30. ‘o\_rs\_vector[25]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x06C’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
31. ‘o\_rs\_vector[26]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x070’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
32. ‘o\_rs\_vector[27]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x074’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
33. ‘o\_rs\_vector[28]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x078’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
34. ‘o\_rs\_vector[29]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x07C’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
35. ‘o\_rs\_vector[30]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x080’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
36. ‘o\_reg\_data’ shall output ‘0’s when ‘i\_addr’ range is between ‘0x028’ and ‘0x02c’
37. ‘o\_reg\_data’ shall output ‘0’s when ‘i\_addr’ range is between ‘0x084’ and ‘0x0fc
38. ‘o\_reg\_data’ shall output ‘0’s if ‘i\_addr’ is ‘0x060’ when ‘Number of Acceptance Filters ’ = ‘0’
39. ‘o\_reg\_data’ shall output ‘0’s if ‘i\_addr’ is ‘0x064’ when ‘Number of Acceptance Filters ’ = ‘0’
40. ‘o\_reg\_data’ shall output ‘0’s if ‘i\_addr’ is ‘0x068’ when ‘Number of Acceptance Filters ’ = ‘0’
41. ‘o\_reg\_data’ shall output ‘0’s if ‘i\_addr’ is ‘0x06c’ when ‘Number of Acceptance Filters ’ = ‘0’
42. ‘o\_reg\_data’ shall output ‘0’s if ‘i\_addr’ is ‘0x070’ when ‘Number of Acceptance Filters ’ = ‘0’
43. ‘o\_reg\_data’ shall output ‘0’s if ‘i\_addr’ is ‘0x074’ when ‘Number of Acceptance Filters ’ = ‘0’
44. ‘o\_reg\_data’ shall output ‘0’s if ‘i\_addr’ is ‘0x078’ when ‘Number of Acceptance Filters ’ = ‘0’
45. ‘o\_reg\_data’ shall output ‘0’s if ‘i\_addr’ is ‘0x07c’ when ‘Number of Acceptance Filters ’ = ‘0’
46. ‘o\_reg\_data’ shall output ‘0’s if ‘i\_addr’ is ‘0x080’ when ‘Number of Acceptance Filters ’ = ‘0’

**Write Operation:**

1. ‘i\_bus\_data’ shall send the data to ‘o\_reg\_w\_bus’ when ‘i\_cs’ is set to ‘1’ and ‘i\_r\_neg\_w’ is set to ‘0’.
2. Module shall read signal from ‘i\_reg\_ack’ and output through ‘o\_ack’
3. ‘i\_cs’ shall be deasserted and reasserted for next write transaction
4. Module shall read signal from ‘i\_r\_neg\_w’ and output through ‘o\_r\_neg\_w’.
5. ‘o\_rs\_vector[0]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x000’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
6. ‘o\_rs\_vector[1]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x004’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
7. ‘o\_rs\_vector[2]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x008’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
8. ‘o\_rs\_vector[3]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x00C’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
9. ‘i\_bus\_data’ shall be ignored when ‘i\_addr’ is ‘0x010’
10. ‘o\_rs\_vector[5]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x014’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
11. ‘i\_bus\_data’ shall be ignored when ‘i\_addr’ is ‘0x018’
12. ‘i\_bus\_data’ shall be ignored when ‘i\_addr’ is ‘0x01C’
13. ‘o\_rs\_vector[8]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x020’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
14. ‘o\_rs\_vector[9]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x024’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
15. ‘o\_rs\_vector[10]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x030’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
16. ‘o\_rs\_vector[11]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x034’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
17. ‘o\_rs\_vector[12]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x038’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
18. ‘o\_rs\_vector[13]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x03c’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
19. ‘o\_rs\_vector[14]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x040’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
20. ‘o\_rs\_vector[15]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x044’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
21. ‘o\_rs\_vector[16]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x048’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
22. ‘o\_rs\_vector[17]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x04c’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
23. ‘i\_bus\_data’ shall be ignored when ‘i\_addr’ is ‘0x050’
24. ‘i\_bus\_data’ shall be ignored when ‘i\_addr’ is ‘0x054’
25. ‘i\_bus\_data’ shall be ignored when ‘i\_addr’ is ‘0x058’
26. ‘i\_bus\_data’ shall be ignored when ‘i\_addr’ is ‘0x05C’
27. ‘o\_rs\_vector[22]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x060’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
28. ‘o\_rs\_vector[23]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x064’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
29. ‘o\_rs\_vector[24]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x068’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
30. ‘o\_rs\_vector[25]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x06C’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
31. ‘o\_rs\_vector[26]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x070’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
32. ‘o\_rs\_vector[27]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x074’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
33. ‘o\_rs\_vector[28]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x078’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
34. ‘o\_rs\_vector[29]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x07C’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
35. ‘o\_rs\_vector[30]’ shall be set to 1 at rising edge of ‘i\_cs’ if ‘i\_addr’ is ‘0x080’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
36. ‘i\_bus\_data’ shall be ignored when ‘i\_addr’ range is between ‘0x028’ and ‘0x02c’
37. ‘i\_bus\_data’ shall be ignored when ‘i\_addr’ range is between ‘0x084’ and ‘0x0fc
38. ‘i\_bus\_data’ shall be ignored if ‘i\_addr’ is ‘0x060’ when ‘Number of Acceptance Filters ’ = ‘0’
39. ‘i\_bus\_data’ shall be ignored if ‘i\_addr’ is ‘0x064’ when ‘Number of Acceptance Filters ’ = ‘0’
40. ‘i\_bus\_data’ shall be ignored if ‘i\_addr’ is ‘0x068’ when ‘Number of Acceptance Filters ’ = ‘0’
41. ‘i\_bus\_data’ shall be ignored if ‘i\_addr’ is ‘0x06c’ when ‘Number of Acceptance Filters ’ = ‘0’
42. ‘i\_bus\_data’ shall be ignored if ‘i\_addr’ is ‘0x070’ when ‘Number of Acceptance Filters ’ = ‘0’
43. ‘i\_bus\_data’ shall be ignored if ‘i\_addr’ is ‘0x074’ when ‘Number of Acceptance Filters ’ = ‘0’
44. ‘i\_bus\_data’ shall be ignored if ‘i\_addr’ is ‘0x078’ when ‘Number of Acceptance Filters ’ = ‘0’
45. ‘i\_bus\_data’ shall be ignored if ‘i\_addr’ is ‘0x07c’ when ‘Number of Acceptance Filters ’ = ‘0’
46. ‘i\_bus\_data’ shall be ignored if ‘i\_addr’ is ‘0x080’ when ‘Number of Acceptance Filters ’ = ‘0’

**Error condition**

MCI\_ER\_01.Module shall read signal from i\_reg\_error and output through ‘o\_error’